This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) A semiconductor device comprising:

a collector layer of first conductive type formed on a semiconductor substrate;

a graft base layer of second conductive type formed in a surface region of the collector layer;

a first base leading-out region of second conductive type formed on the graft base layer;

a second base leading-out region of second conductive type formed on an upper surface and a side surface of the first base leading-out region;

a base layer of second conductive type formed on the collector layer;

an emitter layer of first conductive type formed in a surface region of the base layer; and

an emitter leading-out region formed on the emitter layer,

wherein the base layer is also formed on the second base leading-out region, and at least part of an impurity concentration profile of the second base leading-out region is smaller than an impurity concentration of the first base leading-out region.

2. (Canceled).

3. (Original) A semiconductor device according to claim 1, wherein the first and second base leading-out regions are made of the same material.

4. (Canceled).

5. (Original) A semiconductor device according to claim 1, wherein the base layer is an epitaxial growth layer.

6. (Original) A semiconductor device according to claim 5, wherein the base layer is made of SiGe.

7. – 18. (Canceled).

19. (Previously presented) A semiconductor device, comprising:

a collector layer of first conductive type formed on a semiconductor substrate;

a graft base layer of second conductive type formed in a surface region of the collector layer;

a first base leading-out region of second conductive type formed on the graft base layer;

a second base leading-out region of second conductive type formed on an upper surface and a side surface of the first base leading-out region;

a base layer of second conductive type formed on the collector layer;

an emitter layer of first conductive type formed in a surface region of the base layer; and

an emitter leading-out region formed on the emitter layer,

wherein the first and second base leading-out regions are made of polycrystalline silicon and the base layer is made SiGe, and wherein an impurity concentration of the base layer is lower than that of the first base leading-out region, and an impurity concentration profile of the second base leading-out region is substantially a middle impurity concentration profile between the impurity concentrations of the first base leading-out region which is the lower layer and the base layer which is the upper layer.